Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

FEDL7630-02
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ML7630

13.56MHz wireless charging Rx LSI

■ Overview

The ML7630 is a wireless charging Rx LSI using 13.56MHz carrier frequency, which enables to receive 200mW power wirelessly from a Tx device using the ML7631. The ML7630 also supports the NFC Forum Type3 TAG functions, and a TAG data is read out by the NFC readers including smartphones and tablets.
The ML7630 is equipped with an I²C slave port for host interface and a 10bit SA-ADC for measuring output current to control charging current by software. This is an ideal solution for small rechargeable devices such as headset, ear-pads and wearables.

■ Features

- Charging control
  - Charging power output funcion
    Charging output(LDO): Setting of output voltage and setting of current limitation
    200mW receiving available
  - Abnormaly detection by software control and hardware control

- Communication control
  - NFC Forum Type3 TAG function included
  - Communication speed: 212kbps (13.56MHz/64)
  - 1kbyte data flash for storing TAG data contents

- Host interface(I²C slave)
  - Normal mode(100kbit/s), Fast mode(400kbit/s) available
  - Each internal controller and external HOST microcontroller can access register function

- General Port(PORT)
  - Input/Output port×15ch

- Successive approximation type A/D converter(SA-ADC)
  - Resolution 10bit

- Reset
  - Reset by RESET_N port
  - Power on reset by magnetic field detection
  - Reset by WDT overflow

- Clock
  - Low speed clock : Built-in RC oscillation (32.768kHz) for internal timer
  - High speed clock : From magnetic field(13.56MHz) for internal control logic

- Package
  - WL-CSP34pin

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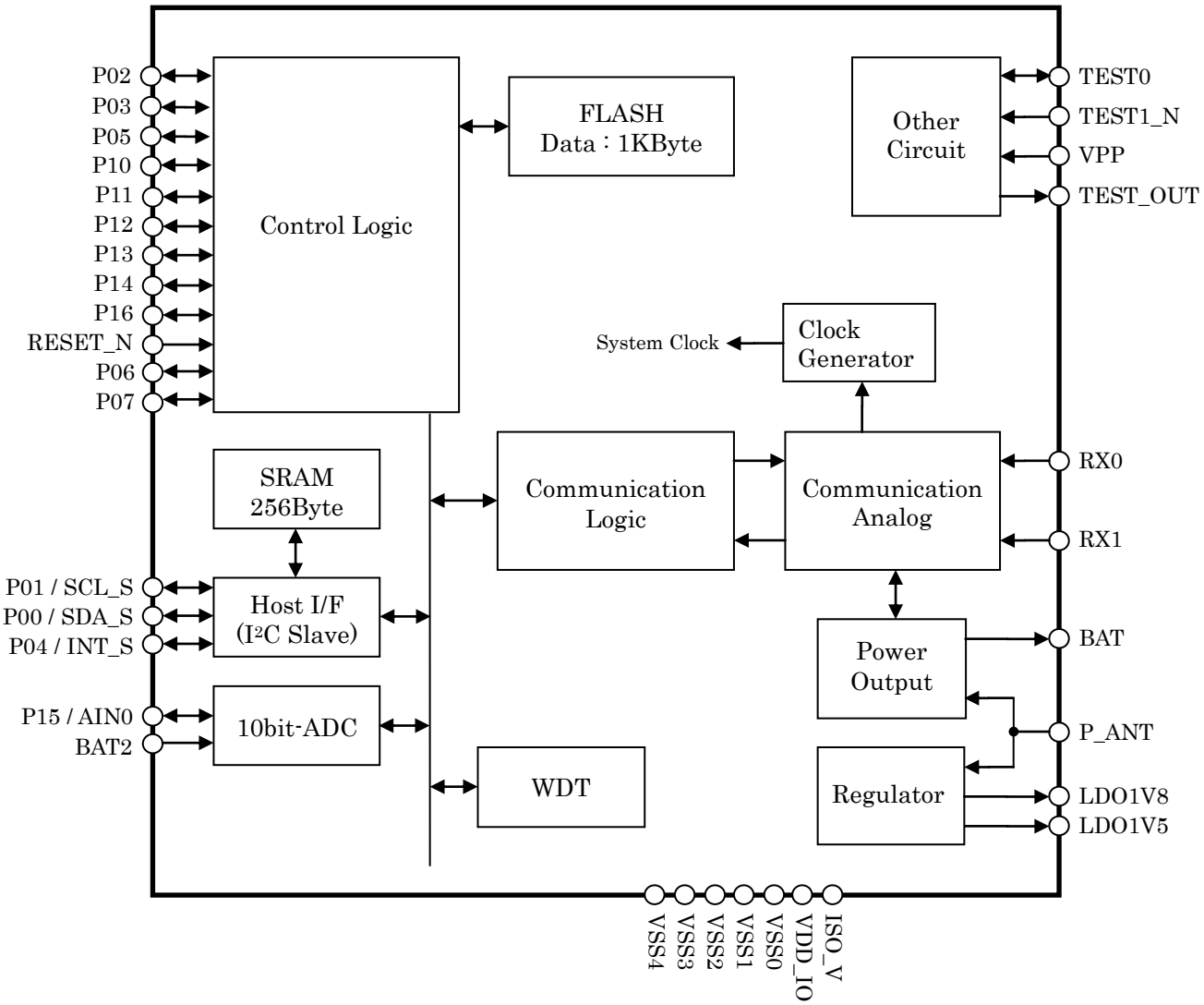
■ Functional block structure



■ Pin assignment

(Top View)

P_ANT	TEST0	P03	RESET_N	P07	P10	A
RX1		TEST1_N	P05	P06	P13	B
RX0	VSS3		P02	TEST_ OUT	VSS1	C
BAT2	BAT	P01 / SCL_S	VPP	P12	VSS0	D
LDO1V8	LDO1V5	P00 / SDA_S	P11	P14	VDD_IO	E
VSS4	ISO_V	VSS2	P04 / INT_S	P15 / AIN0	P16	F
1	2	3	4	5	6	

(Bottom View)

P16	VDD_IO	VSS0	VSS1	P13	P10	6
P15 / AIN0	P14	P12	TEST_ OUT	P06	P07	5
P04 / INT_S	P11	VPP	P02	P05	RESET_N	4
VSS2	P00 / SDA_S	P01 / SCL_S		TEST1_N	P03	3
ISO_V	LDO1V5	BAT	VSS3		TEST0	2
VSS4	LDO1V8	BAT2	RX0	RX1	P_ANT	1
F	E	D	C	B	A	

■ Pin description

- Power · GND · reference voltage pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active level	Description	Process in not use
D6	VSS0	−	−	−	Ground	−
C6	VSS1					
F3	VSS2					
C2	VSS3					
F1	VSS4					
E6	VDD_IO	−	−	−	Logic IO voltage	−
E2	LDO1V5	H(A)	O_A	−	Core 1.5V voltage output	−
E1	LDO1V8	H(A)	O_A	−	ADC 1.8V voltage output	−
A1	P_ANT	−	−	−	Rectify output	−
F2	ISO_V	−	−	−	Logic IO voltage (for host communication)	−
D2	BAT	Z	O_A	−	Charging voltage output	−
D1	BAT2	−	I_A	−	Battery voltage monitoring/Flash writing power	GND

- Analog signal pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active level	Description	Process in not use
C1	RX0	−	I_A	−	Antenna（Plus） / Data receiving	−
B1	RX1	−	I_A	−	Antenna（Minus） / Data receiving	−

- Reset pin

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description	Process in not use
A4	RESET_N	PU	I	VDD_IO	L	Reset input	Open

- General pins

Since the settings differ depending on the FW Ver., refer to the application note for details.

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description
E3	P00 / SDA_S	Z	I/O	ISO_V	−	Input/Output port HostIF(I^2C slave) Data
D3	P01 / SCL_S	Z	I/O	ISO_V	−	Input/Output port HostIF(I^2C slave) Clock
C4	P02	Z	I/O	VDD_IO	−	Input/Output port
A3	P03	Z	I/O	VDD_IO	−	Input/Output port
F4	P04 / INT_S	Z	I/O	ISO_V	−	Input/Output port HostIF INToutput
B4	P05	Z	I/O	VDD_IO	−	Input/Output port
B5	P06	Z	I_{DA}/O	VDD_IO	−	Input/Output port
A5	P07	Z	I_{DA}/O	VDD_IO	−	Input/Output port
A6	P10	Z	I/O	VDD_IO	−	Input/Output port
E4	P11	Z	I/O	ISO_V	−	Input/Output port
D5	P12	Z	I/O	ISO_V	−	Input/Output port
B6	P13	Z	I/O	VDD_IO	−	Input/Output port
E5	P14	Z	I/O	VDD_IO	−	Input/Output port
F5	P15 / AIN0	Z	I_{DA}/O	VDD_IO	−	Input/Output port AD input
F6	P16	Z	I/O	VDD_IO	−	Input/Output port

- Test pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active level	Description	Process in not use
A2	TEST0	PD	I/O	VDD_IO	H	For test/For debugger	Open
B3	TEST1_N	PU	I	VDD_IO	L	For test/For debugger	Open
D4	VPP	−	I_A	−	−	Power supply for Flash test	Open
C5	TEST_OUT	L(A)	O	VDD_IO	−	Test output port	Open

(*1) In reset state :

Pin state definition in reset state	L(O)	:	“L” level output
	H(O)	:	“H” level output
	L(A)	:	Analog “L” level output
	H(A)	:	Analog “H” level output
	PU	:	Pull-Up
	PD	:	Pull-Down
	Z	:	Floating state

(*2) I/O : For I/O definition, using under abbreviation

I/O definition	I_A	:	Analog input
	O_A	:	Analog output
	I	:	Digital input
	I/O	:	Bi-directional pin
	I_{DA}/O	:	Bi-directional pin, Input are digital and analog shared
	O	:	Digital output

■ Electrical characteristics

- Absolue maximum ratings

Item	Symbol	Condition	Rating	Unit
Power voltage	VDD_IO	Ta=25°C	-0.3 to +6.5	V
	ISO_V	Ta=25°C	-0.3 to +6.5	V
	P_ANT	Ta=25°C	-0.3 to +6.5	V
	BAT2	Ta=25°C	-0.3 to +6.5	V
Core power voltage	LDO1V5	Ta=25°C	-0.3 to +2.0	V
Analog power voltage	LDO1V8	Ta=25°C	-0.3 to +6.5	V
Input voltage	V_{DIN}	Ta=25°C, Digital port	-0.3 to V_{DD}+0.3	V
		Ta=25°C, RX0/RX1	12	V
Input current	Ii	Ta=25°C, Digital port	-10 to +10	mA
	I_{P_ANT}	Ta=25°C	100	mA
Output voltage	V_{DO}	Ta=25°C, Digital port	-0.3 to V_{DD}+0.3	V
Digital output current	I_{DO}	Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{stg}	–	-55 to +150	°C

V_{DD} : Refer to Pin Description table, in case "Supply Power" column equals "VDD_IO", VDD is VDD_IO voltage and column equals "ISO_V", VDD is ISO_V voltage.

- Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD_IO	–	1.8	–	5.5	V
	ISO_V	–	1.8	–	5.5	V
	P_ANT	Normal	2.0	5.0	5.5	V
		Charging	–	–	5.5	V
Input current	P_ANT	Normal	0.5	–	–	mA
		Charging	–	–	80	mA
Operating temperature	T_{a1}	Normal	-40	+25	+85	°C
	T_{a2}	Charging	-10	+25	+50	°C
LDO1V5 outside Capacitor	C_{LDO1V5}	–	Typ -10%	2.2	Typ +10%	µF
P_ANT outside Capacitor	C_{PANT}	–	Typ -10%	2.2	Typ +10%	µF
LDO1V8 outside Capacitor	C_{LDO1V8}	–	Typ -10%	0.47	Typ +10%	µF
VDD_IO outside Capacitor	C_{VDDIO}	–	Typ -10%	0.1	Typ +10%	µF
ISO_V outside Capacitor	C_{ISOV}	–	Typ -10%	0.1	Typ +10%	µF
Antenna input frequency	F_{ANT}	–	Typ -0.05%	13.56	Typ +0.05%	MHz

- Flash memory operating conditions

Item	Symbol	Condition	Range	Unit
Operating temperature (Ambience)	T_{OP}	write/erase	-20 to +60	°C
Operating voltage	P_ANT	Write/erase	2.7 to 5.5	V
Write time	C_{EPD}	–	10,000	times
Erase unit	–	Sector erase	1	KB
Erase time (Maximum)	–	Block erase / Sector erase	100	ms
Write time	–	–	1 word (2 byte)	–

- RF charactaristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Level	V_{RX1}	RX0/RX1	2.0	–	5.5	V
Input data amplitude	V_{RX2}	RX0/RX1	50	–	–	mV
Communication speed	F_{RX}	RX0/RX1	–	212	–	kbps
Load modulation resistance	R_{MOD}	RX0/RX1	105	–	220	Ω

- Power suppycharactaristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
BAT pin output voltage	V_{BAT}	No load	–	5.0	––	V
BAT pin Load Characteristic	V_{BAT_LOAD}	45mA load	V_{BAT}-0.5	–	–	V

Refer to the application note for how to set the BAT pin output voltage.

- Notification charactaristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
P_ANT limiter	V_{PANT1}	Norma	–	–	5.5	V
	V_{PANT2}	In case of abnormality notice	–	3.0	–	V

- Oscillation characteristic

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Low speed embedded RC oscillator frequency *1	f_{LCR}		-5%	32.768	+5%	kHz

*1：1024 cycle average

- SA-ADC characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	–	–	10	–	bit
Integral non-linearity error	INL	LDO1V8=1.8V	6	–	+6	LSB
Differential non-linearity error	DNL	LDO1V8=1.8V	-6	–	+6	LSB
Zero scale error	ZSE	–	-6	–	+6	LSB
Full scale error	FSE	–	-6	–	+6	LSB
Input impedance	RI	–	–	6k	–	Ω
SA-ADC reference voltage	V_{REF}	LDO1V8=V_{REF}	–	1.8	–	V

- Reset characteristics

(VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RESET_N pulse width	P_{RST}	–	200	–	–	µs
RESET_N noise removal Pulse width	P_{NRST}	–	–	–	0.3	µs

- ACcharacteristics (I^2C bus interface: Standard mode 100 kHz)

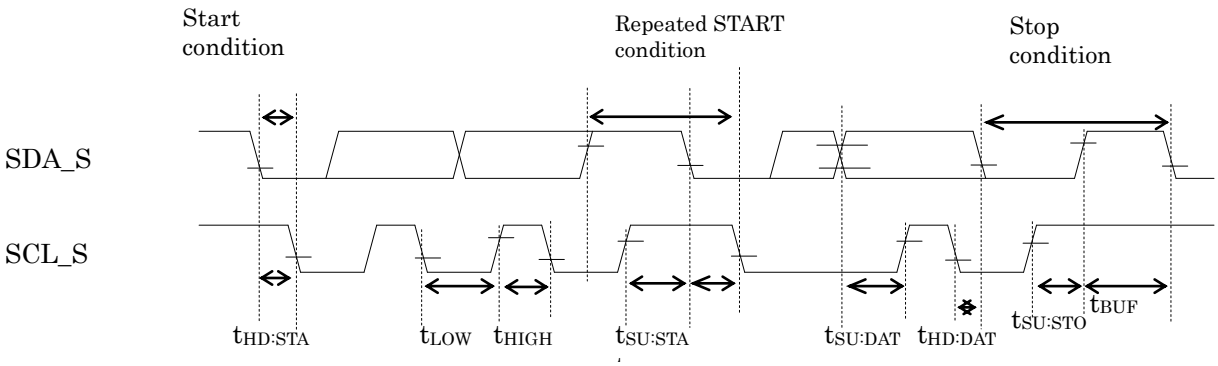
(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	100	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL_S "L" level time	t_{LOW}	–	4.7	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus free time	t_{BUF}	–	4.7	–	–	µs

- AC characteristics (I^2C bus interface: Fast mode 400 kHz)

(VDD_IO/ISO_V=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	400	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL_S "L" level time	t_{LOW}	–	1.3	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus free time	t_{BUF}	–	1.3	–	–	µs



If powering off ISO_V of this LSI, it disables communications of other devices on the I^2C bus.
If there is a power supply of ISO_V of this LSI even if powering off P_ANT of this LSI, SDA_S/SCL_S maintains Hi-z state.

- IO characteristics

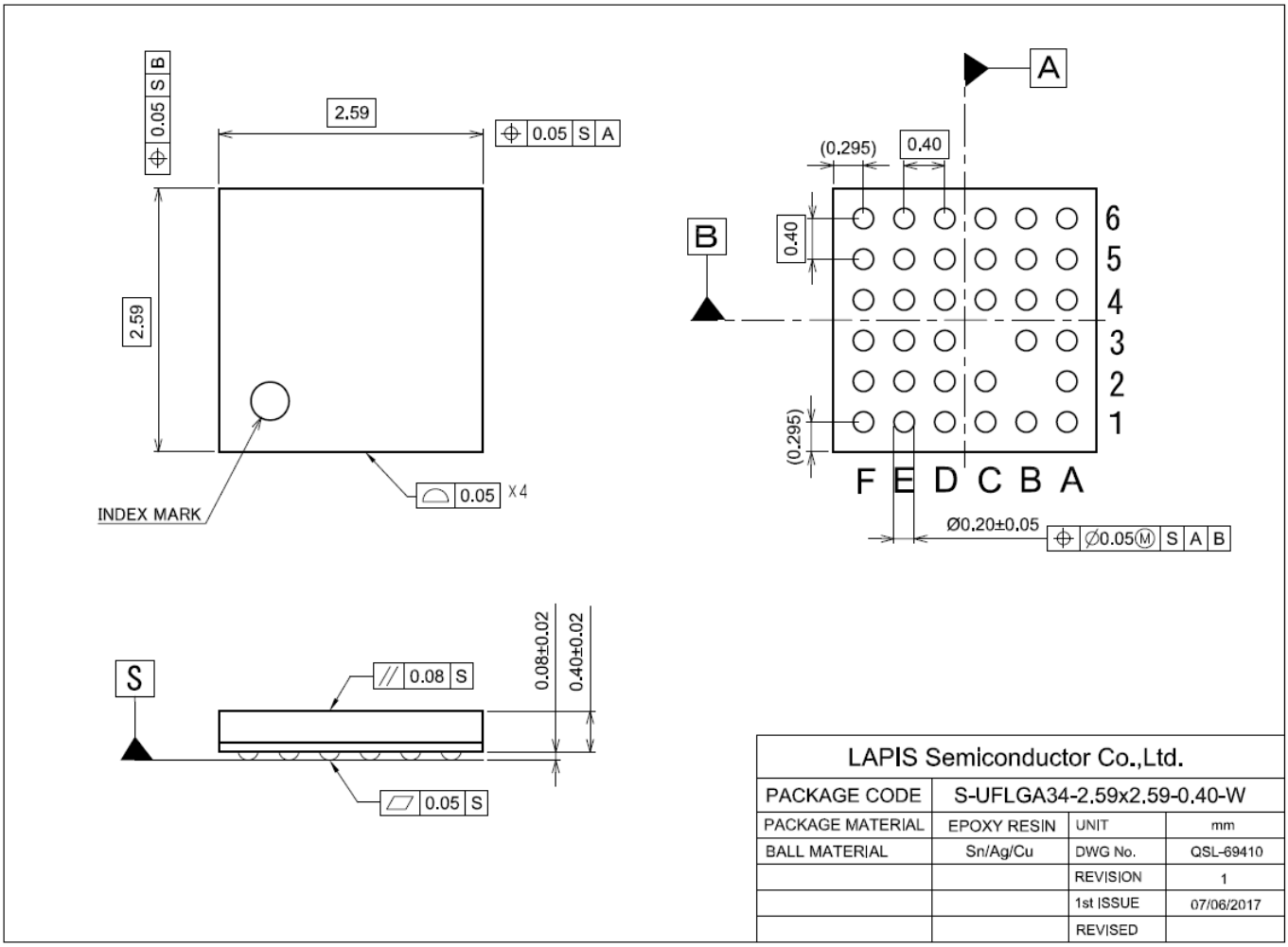
(Unless otherwise specified, VDD_IO=1.8 to 5.5V, P_ANT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1 (P00-P07, P10-P16)	VOH1	IOH=-1.0mA	V_{DD}-0.5	–	–	V
	VOL1	IOL=+0.5mA	–	–	0.4	V
Output voltage 2 (P00-P07, P10-P16) (LED pin)	VOL2	2.7V≤V_{DD}≤5.5V IOL=+5.0mA	–	–	0.6	V
		IOL=+2.0mA	–	–	0.4	V
Output voltage 3 (SCL_S,SDA_S) (I^2C pin)	VOL3	IOL3= +3mA (I^2Cspec) (VDD_IO ≥2V, ISO_V≥2V)	–	–	0.4	V
Output voltage 4 (SCL_S,SDA_S) (I^2C pin)	VOL4	IOL4= +2mA (I^2Cspec) (VDD_IO <2V, ISO_V<2V)	–	–	V_{DD}×0.2	V
Output leakage 1 (P00-P07, P10-P16, SCL_S, SDA_S)	IOOH1	VOH=V_{DD} (at high impedance)	–	–	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	–	–	μA
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=V_{DD}	–	–	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	20	300	900	μA
	IIL2	VIL2=VSS	-1	–	–	μA
Input current 3 (P00-P07, P10-P16)	IIH3	VIH3=V_{DD} (In pull down)	1	15	200	μA
	IIL3	VIL3=VSS (In pull up)	-200	-15	-1	μA
	IIH3Z	VIH3=V_{DD} (at high impedance)	–	–	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	–	–	μA
Input voltage 1 (RESET_N, TEST0, TEST1_N, P00-P07, P10-P16)	VIH1	–	0.7×V_{DD}	–	V_{DD}	V
	VIL1	–	0	–	0.3×V_{DD}	V
Input pincapacitance (RESET_N, TEST0, TEST1_N, P00-P07, P10-P16)	CIN	f=10kHz Vrms=50mV Ta=25°C	–	10	–	pF
Leak current	I_{ISOV}	Voltage supply to the ISO_V terminal, no magnetic field input	–	100	–	nA

V_{DD} : Refer to Pin Description table, in case "Supply Power" column equals "VDD_IO", VDD is VDD_IO voltage and column equals "ISO_V", VDD is ISO_V voltage.

Typ. standard is at Ta=25°C, VDD_IO=3.0V

■ Package dimensions



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	S-UFLGA34-2.59x2.59-0.40-W		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
BALL MATERIAL	Sn/Ag/Cu	DWG No.	QSL-69410
		REVISION	1
		1st ISSUE	07/06/2017
		REVISED	

■ Revision historys

Document No.	Issue date	Page		Change contents
		Previous edition	Current edition	
PEDL7630-01	Oct. 25, 2016	–	–	Preliminary edition 1
FEDL7630-01	Mar. 23, 2018	–	–	Final edition 1
FJDL7630-02	Jan. 15, 2019	9	9	Revise IO-pin description
	Nov. 18, 2019	1 2 3 4	1 2 3 4	Delet Unused block
		4 5	4 5	Add Reset pin category Rename Other pins to General pins Added note for application note to general pin
		11 12	-	Delete Sample Circuit (Described in the application note because it depends on the FW)
		3	3	Add TOP VIEW
		4	4	Add description when BAT2 is not used
		2	2	Change the connection destination of BAT2 to ADC
		7	7	Revise BAT output voltage description

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