FEDL-7661-01
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ML7661

13.56MHz wireless charging Tx LSI

1. Overview

ML7661 is a 13.56MHz wireless power transmission device. ML7661 realizes a wireless power supply system by combining with the power receiving device ML7660, and can output 1W for power transmission.
The ML7661 has a communication command generation function for communicating with the power receiving device ML7660, an external transistor control function for supplying 1W, a function for variably controlling the transmission amount to optimize the transmission power, and a function to detect abnormalities when the ML7660 is attached/detached or power is transmitted. All of these functions are included in the 40-pin WQFN package(6.0 mm square), and the ML7661 is the best LSI for wireless power supply of small devices.In addition, the operating voltage is 5V, and it can be driven from a USB power source such as a mobile battery.Furthermore, ML7661 is equipped with a host interface (SPI / I²C slave) function and a serial interface (SPI / I²C master, UART) function, and it is possible to update configuration data from an external MCU and control various sensors.

2. Features

- Charging control
  - Built-in 13.56MHz power transmission control circuit
    1W power transmission transistor control output
  - Abnormaly detection by software and hardware control

- NFC communication control
  - Equipped with a command generation function for communication with ML7660
  - Communication speed: 212kbps, 424kbps
  - 2Kbyte data flash for storing user data

- Host interface
  - 1ch Serial interface (Slave), and selectable from SPI or I²C
  - Register function accessible from the host MCU
  - Built-in 512byte FIFO

- Serial interface
  - 1ch SPI interface(Master)
  - 1ch I²C interface(Master)
  - 1ch UART interface (2-wire, Full-duplex communication mode)

- General Port(PORT)
  - Input/Output×13ch

- Successive approximation type A/D converter (SA-ADC)
  - Resolution 10bit

- Reset
  - Reset by RESET_N port
  - Power on reset
  - Reset by WDT overflow

ROHM SEMICONDUCTOR

- Clock
  - — Low speed clock
    Built-in RC oscillation(32.768kHz)
  - — High speed clock
    Crystal oscillator (27.12MHz)

- Package
  - — WQFN40pin(P-WQFN40-0606-0.50-63)

- CPU
  - — 16-bit RISC CPU（CPU：nX-U16/100）
  - — Built-in On-chip debug function
  - — Minimum instruction execution time
    - ✧ 147.5ns（@6.78MHz system clock）

- Internal memory
  - — Memory size

Flash*	SRAM	Other RAM
Program：32K byte Data：2K byte	6K byte（Work RAM） 1K byte(For debugger trace function)	256 byte（For NFC） 512 byte (For Host interface)

*: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.
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- Interrupt controller (INTC)
  - — 1 non-maskable interrupt source (Internal source: WDT)
  - — 26 maskable interrupt sources(Internal source: 18, External source: 8）
  - — Software interrupt(SWI): Max. 64 sources
  - — Selectable edge and sampling for external interrupt and comparator
  - — Four step unterrupt levels

- Timer
  - — 8bit×8ch (16-bit configuration is possible using 2ch)
  - — Built-in Repeat mode, One shot mode is available
  - — Timer start/stop function by software

- Watchdog timer(WDT)
  - — Non-maskable interrupt and Reset
    1st overflow: generate interrupt, 2nd overflow: generate reset or host notification
  - — Free-run
  - — Overflow period: 4 selectable(125ms, 500ms, 2s, 8s) at LSCLK=32.768kHz
  - — Stop function

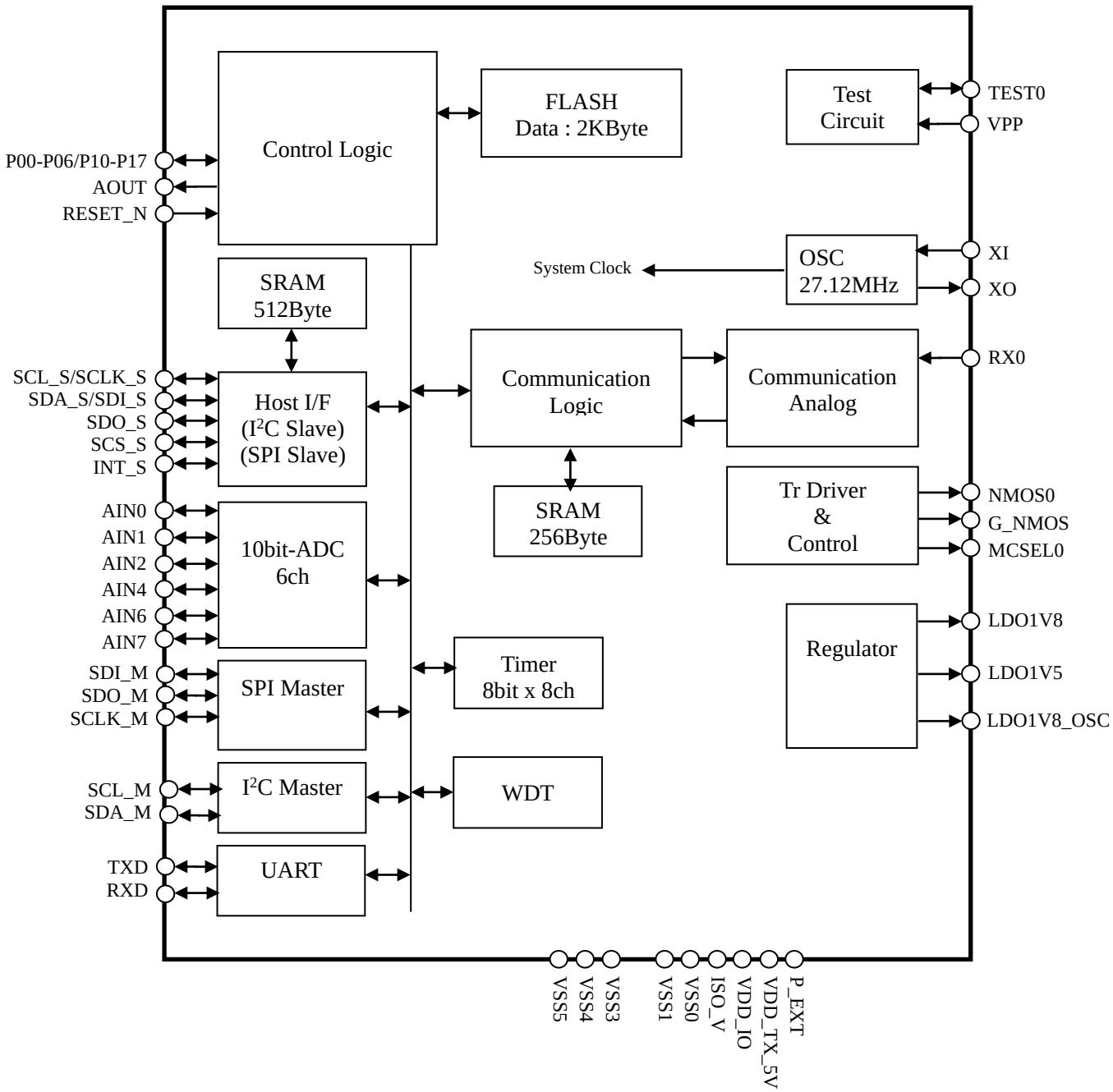
- I^2C bus interface (I^2C Master)
  - Normal mode (100kbit/s), Fast mode (400kbit/s) available

- SPI interface (SPI Master)
  - Selectable from MSB/LSB first
  - Selectable from 8-bit length or 16-bit length
  - Selectable clock phase and polarity

- UART
  - Full-duplex communication mode
  - Communication speed: 4800 to 115200bps
  - Programable interface (Data length, Parity and Stop bit can be selected)

- Power management
  - Clock division function
    System clock supports 6.78MHz, 3.39MHz, 1.7MHz, 848kHz, 424kHz, 212kHz and 106kHz
  - Clock stop function
    HALT mode to stop only CPU
    HALT-H mode to stop CPU and high speed clock

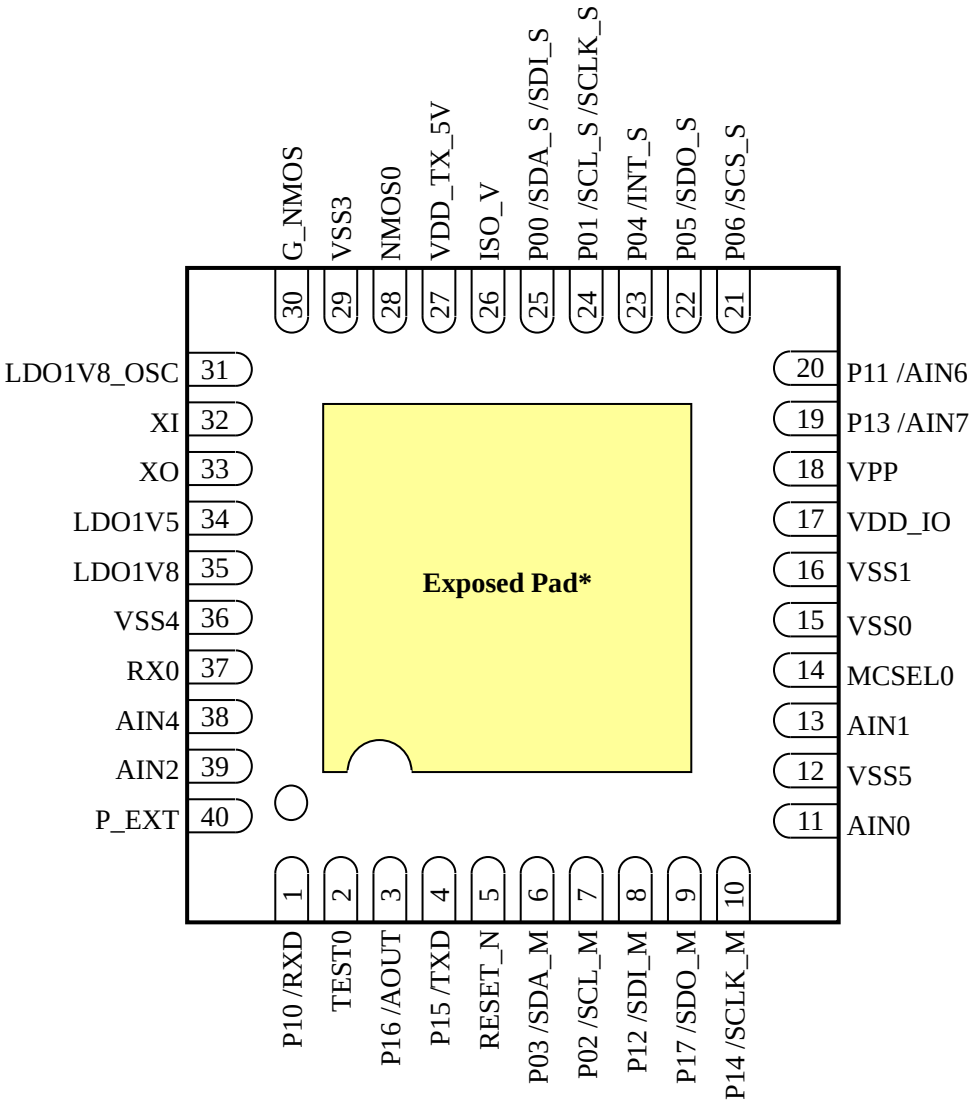
3. Functional block structure



4. Pin assignment

WQFN 40pin

TOP VIEW



*Solder the exposed pad onto the PCB

5. Pin description

5.1 Power GND reference voltage pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Active Level	Description	Process in not use
15	VSS0	–	–	–	Ground (VSS0 to VSS5 are connected inside the LSI, respectively)	–
16	VSS1					
29	VSS3					
36	VSS4					
12	VSS5					
17	VDD_IO	–	–	–	Logic IO voltage	–
34	LDO1V5	H(A)	OA	–	Core 1.5V voltage output	–
35	LDO1V8	H(A)	OA	–	ADC 1.8V voltage output	–
31	LDO1V8_OSC	H(A)	OA	–	27.12MHz oscillator 1.8V voltage output	–
40	P_EXT	–	–	–	External Power supply (5V)	–
26	ISO_V	–	–	–	Logic IO voltage (for host communication)	–
27	VDD_TX_5V	–	–	–	Power supply for driver (5V)	–

* Connect ISO_V to VDD_IO on the board

5.2 Analog signal pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
37	RX0	–	IA	–	–	RF Data receiving	–
30	G_NMOS	PD	OA	VDD_TX_5V	–	N transistor bias output for charging	–
28	NMOS0	Z	OA	VDD_TX_5V	–	N transistor driver for charging	–

5.3 Clock pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
32	XI	I	I	LDO1V8_OSC	–	27.12MHz oscillation pin	–
33	XO	O	O	LDO1V8_OSC	–	27.12MHz oscillation pin	–

5.4 Other Pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
5	RESET_N	PU	I	VDD_IO	L	Reset input /For debugger	Open
25	P00 / SDA_S / SDI_S	Z	I/O	ISO_V	–	Input/Output port HostIF(I^2C slave) data input/output HostIF(SPI slave) data input	Open
24	P01 / SCL_S / SCLK_S	Z	I/O	ISO_V	–	Input/Output port HostIF(I^2C slave) clock input HostIF(SPI slave) clock input	Open
7	P02 / SCL_M	Z	I/O	ISO_V	–	Input/Output port I^2C master clock output	Open
6	P03 / SDA_M	Z	I/O	ISO_V	–	Input/Output port I^2C master data input/output	Open
23	P04 / INT_S	Z	I/O	ISO_V	–	Input/Output port HostIF INT output	Open

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
22	P05 / SDO_S	Z	I/O	ISO_V	–	Input/Output port HostIF(SPI slave) data output	Open
21	P06 /SCS_S	Z	I/O	ISO_V	–	Input/Output port HostIF(SPI slave) select signal	Open
11	AIN0	Z	I_A	VDD_IO	–	AD input 0	Open
13	AIN1	Z	I_A	VDD_IO	–	AD input 1	Open
39	AIN2	Z	I_A	P_EXT	–	AD input 2	Open
38	AIN4	Z	I_A	P_EXT	–	AD input 4	Open
1	P10 / RXD	PU	I/O	VDD_IO	–	Input/Output port UART data input	Open
20	P11 / AIN6	Z	I_{DA}/O	ISO_V	–	Input/Output port /AD input 6	Open
8	P12 / SDI_M	Z	I/O	ISO_V	–	Input/Output port SPI master data input	Open
19	P13 / AIN7	Z	I_{DA}/O	VDD_IO	–	Input/Output port /AD input 7	Open
10	P14 / SCLK_M	Z	I/O	ISO_V	–	Input/Output port SPI master clock output	Open
4	P15 / TXD	Z	I/O	VDD_IO	–	Input/Output port UART data output	Open
3	P16 / AOUT	Z	I/O_{DA}	VDD_IO	–	Input/Output port Analog monitor output	Open
9	P17 / SDO_M	Z	I/O	ISO_V	–	Input/Output port SPI master data output	Open
14	MCSEL0	PU	O	VDD_IO	–	Matching capacitor select signal	Open

5.5 Test pins

PIN No.	Pin name	In reset (*1)	I/O (*2)	Supply power	Active Level	Description	Process in not use
2	TEST0	Z	I/O	VDD_IO	L	For debugger	Pull-Up
18	VPP	–	I_A	–	–	Power supply for Flash test	Open

(*1) In reset state :

Pin state definition in reset state	L(O)	:	“L” level output
	H(O)	:	“H” level output
	L(A)	:	Analog “L” level output
	H(A)	:	Analog “H” level output
	PU	:	Pull-Up
	PD	:	Pull-Down
	Z	:	Floating state

(*2) I/O : For I/O definition, using under abbreviation

I/O definition	I_A	:	Analog input
	O_A	:	Analog output
	I	:	Digital input
	I/O	:	Bi-directional pin
	I_{DA}/O	:	Bi-directional pin, Input are digital and analog shared
	I/O_{DA}	:	Bi-directional pin, Output are digital and analog shared
	O	:	Digital output

6. Electrical characteristics

6.1 Absolute maximum ratings

Item	Symbol	Condition	Rating	Unit
Power voltage（Digital IO）	VDD_IO	Ta=25°C	-0.3 to +6.5	V
	ISO_V	Ta=25°C	-0.3 to +6.5	V
Regulator Input voltage	P_EXT	Ta=25°C	-0.3 to+6.5	V
Power voltage (Power transmission)	VDD_TX_5V	Ta=25°C	-0.3 to +6.5	V
Core power voltage / Crystal oscillator voltage	LDO1V5	Ta=25°C	-0.3 to +2.0	V
Analog power voltage	LDO1V8	Ta=25°C	-0.3 to +6.5	V
27.12MHz oscillator power voltage	LDO1V8_OSC	Ta=25°C	-0.3 to +6.5	V
Input voltage	V_{DIN}	Ta=25°C, Digital port	-0.3 to V_{DD_IO}+0.3	V
		Ta=25°C, RX0	-0.3 to +6.5	V
Input current	Ii	Ta=25°C, Digital port	-10 to +10	mA
Output voltage	V_{DO}	Ta=25°C, Digital port	-0.3 to V_{DD_IO}+0.3	V
Digital output current	I_{DO}	Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	1	W
Storage temperature	T_{stg}	—	-55 to +150	°C

6.2 Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD_IO	—	1.8	—	5.5	V
	ISO_V	Connect with VDD_IO on the board	1.8	—	5.5	V
	P_EXT	—	4.5	5.0	5.5	V
	VDD_TX_5V	—	4.5	5.0	5.5	V
Operating temperature	T_{a1}	Communication	-40	+25	+85	°C
	T_{a2}	Charging	T.B.D.	+25	T.B.D.	°C
Crystal oscillator frequency	f_{XTL}		Typ -0.05%	27.12	Typ +0.05%	MHz
Crystal oscillator load capacitance	C_{DL} C_{GL}	NIHON DEMPA KOGYO Co., Ltd. NX2016SA(CL=6pF)	Typ -1%	8	Typ +1%	pF
	C_{DL} C_{GL}	NIHON DEMPA KOGYO Co., Ltd. NX2016SA(CL=8pF)	Typ -1%	12	Typ +1%	pF
	C_{DL} C_{GL}	KYOCERA Corporation CX1210SB(CL=6pF)	Typ -1%	8	Typ +1%	pF
	C_{DL} C_{GL}	KYOCERA Corporation CX2016DB(CL=8pF)	Typ -1%	12	Typ +1%	pF
	C_{DL} C_{GL}	TXC SMD SEAM SEALING XTAL 2.0 x 1.6(CL=8pF)	Typ -1%	12	Typ +1%	pF
LDO1V5 outside Capacitor	C_{LDO1V5}	—	Typ -10%	2.2	Typ +10%	µF
P_EXT outside Capacitor	C_{PEXT}	—	Typ -10%	2.2	Typ +10%	µF
LDO1V8 outside Capacitor	C_{LDO1V8}	—	Typ -10%	0.47	Typ +10%	µF
LDO1V8_OSC outside Capacitor	$C_{LDO1V8OSC}$	—	Typ -10%	0.47	Typ +10%	µF
VDD_IO outside Capacitor	C_{VDDIO}	—	Typ -10%	0.1	Typ +10%	µF
VDD_TX_5V outside Capacitor	C_{TX5V}	—	Typ -10%	2.2	Typ +10%	µF
AIN input voltage	V_{AIN}	AIN0,AIN6,AIN7	0	—	1.8	V

6.3 Flash memory operating conditions

項目	記号	条件	範囲	単位
Operating temperature (Ambience)	T_{OP}	write/erase	-20 to +60	°C
Operating voltage	P_EXT	write/erase	4.5 to 5.5	V
Rewrite count	C_{EPD}	Program Flash	100	times
		Data Flash	10,000	times
Erase unit	–	Sector erase (Program Flash)	1	KB
		Sector erase (Data Flash)	128	B
Erase time (Maximum)	–	Sector erase	50	ms
Write unit	–	Program Flash	4 bytes	–
		Data Flash	1 byte	–

6.4 Power transmission characteristics

(VDD_IO=1.8 to 5.5V, VDD_TX_5V=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
nmos0 output frequency	F_{TX}	ー	ー	13.56	ー	MHz

6.5 Ocsillation characteristics

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Low speed embedded RC oscillator frequency *1	f_{LCR}	ー	-10%	32.768	+10%	kHz

*1：1024 cycle average

6.6 SA-ADC characteristics

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	ー	–	10	–	bit
Integral non-linearity error	INL	LDO1V8=1.8V	-6	–	+6	LSB
Differential non-linearity error	DNL	LDO1V8=1.8V	-6	–	+6	LSB
Zero scale error	ZSE	ー	-6	–	+6	LSB
Full scale error	FSE	ー	-6	–	+6	LSB
Input impedance	RI	ー	–	6k	–	Ω
SA-ADC reference voltage	V_{REF}	LDO1V8=V_{REF}	–	1.8	–	V

6.7 Reset characteristics

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
RESET_N pulse width	P_{RST}	—	2	–	–	ms
RESET_N noise removal Pulse width	P_{NRST}	—	–	–	0.3	μs

6.8 DAC characteristics

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage range	V_{DAC}	dac_level=0 to 511	–	4	–	V
Output voltage step width	V_{STEP}	—	–	–	10	mV
Output volrage temperature characteristics	V_{temp}	Max-Min	–	–	1	dB

6.9 AC characteristics (I^2C Bus Interface)

● Standard Mode 100kHz

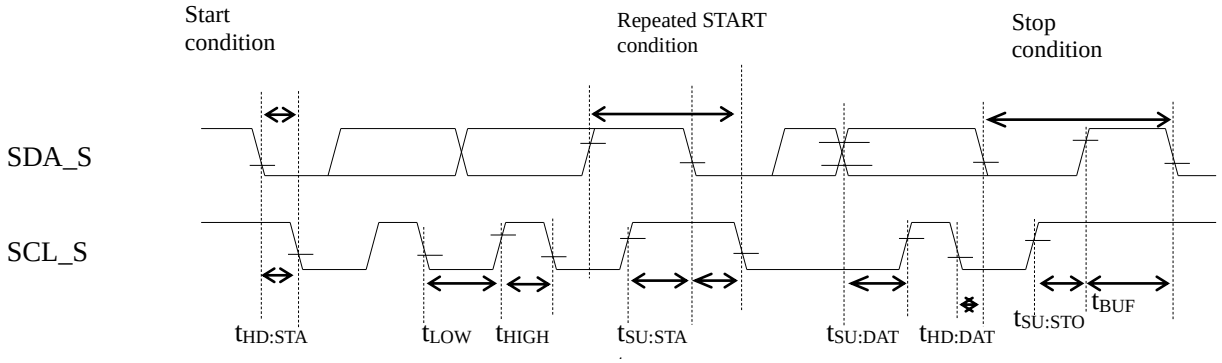
(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	100	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL_S "L" level time	t_{LOW}	–	4.7	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus free time	t_{BUF}	–	4.7	–	–	µs

● Fast Mode 400kHz

(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL_S clock frequency	f_{SCL}	–	–	–	400	kHz
SCL_S hold time (start/repeated start condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL_S "L" level time	t_{LOW}	–	1.3	–	–	µs
SCL_S "H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL_S setup time (repeated start condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA_S hold time	$t_{HD:DAT}$	–	0	–	–	µs
SDA_S setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SDA_S setup time (P: Stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus free time	t_{BUF}	–	1.3	–	–	µs

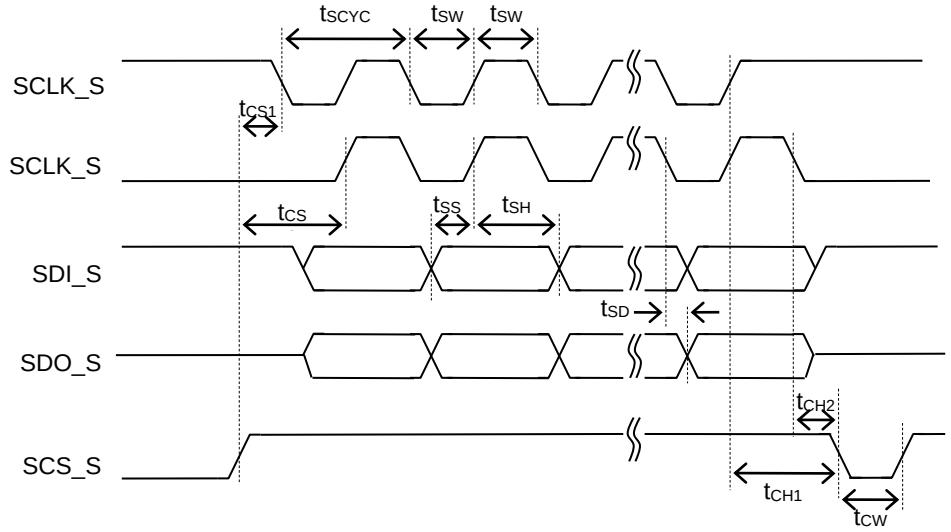


If powering off this LSI, it disables communications of other devices on the I^2C bus.

6.10 AC characteristics (Host Interface : SPI slave)

(VDD_IO/ISO_V=1.8 to 5.5V, P_EXT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_S input cycle	t_{SCYC}	–	500	–	–	ns
SCLK_S input pulse width	t_{SW}	–	200	–	–	ns
SCS_S setup time	t_{CS1}	–	80	–	–	ns
	t_{CS2}	–	80	–	–	ns
SCS_S hold time	t_{CH1}	–	80	–	–	ns
	t_{CH2}	–	80	–	–	ns
SCS_S input pulse width	t_{CW}	–	80	–	–	ns
SDO_S output delay time	t_{SD}	–	–	–	240	ns
SDI_S input setup time	t_{SS}	–	80	–	–	ns
SDI_S input hold time	t_{SH}	–	80	–	–	ns

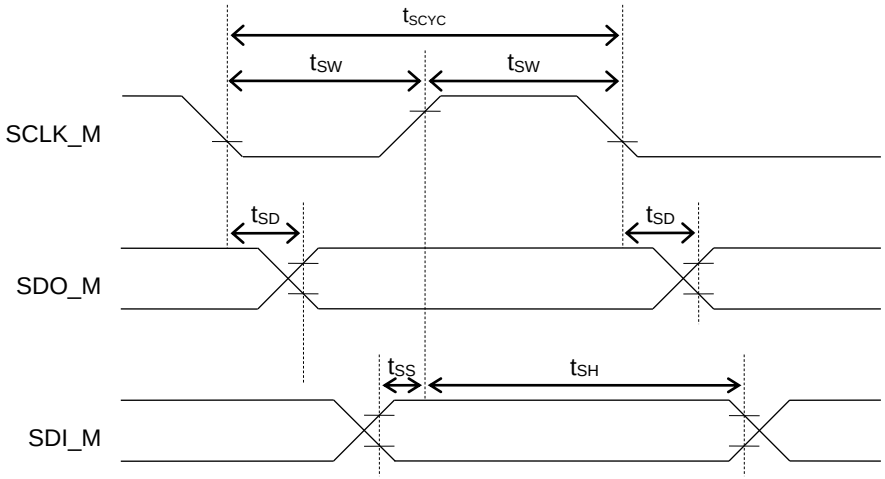


6.11 AC characteristics (SPI master)

(VDD_IO/ISO_V=1.8 to 5.5V, P_EXT=2.0 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK_M output cycle	t_{SCYC}	–	–	SCLK*1	–	s
SCLK_M output pulse width	t_{SW}	–	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SDO_M output delay time	t_{SD}	–	–	–	100	ns
SDI_M input setup time	t_{SS}	–	100	–	–	ns
SDI_M input hold time	t_{SH}	–	60	–	–	ns

*1 : The Period of the internal clock selected by the interface register



6.12 IO characteristics

(Unless otherwise specified,VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage 1 (P00-P07, P10-P17)	VOH1	IOH=-1.0mA	V_{DD_IO} -0.5	–	–	V
	VOL1	IOL=+0.5mA	–	–	0.4	V
Output voltage 2 (P00-P07, P10-P17) (LED mode selected)	VOL2	2.7V ≤ VDD_IO ≤ 5.5V IOL=+5.0mA	–	–	0.6	V
		IOL=+2.0mA	–	–	0.4	V
Output voltage 3 (P00-P03) (I^2C mode selected)	VOL3	IOL3= +3mA (I^2C spec) (VDD_IO ≥ 2V)	–	–	0.4	V
Output voltage 4 (P00-P03) (I^2C mode selected)	VOL4	IOL4= +2mA (I^2C spec) (VDD_IO < 2V)	–	–	V_{DD_IO} ×0.2	V
Output leakage 1 (P00-P07, P10-P17)	IOOH1	VOH=VDD_IO (at high impedance)	–	–	1	μA
	IOOL1	VOL=VSS (at high impedance)	-1	–	–	μA
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=VDD_IO	–	–	1	μA
	IIL1	VIL1=VSS	-900	-300	-20	μA
Input current 2 (TEST0)	IIH2	VIH2=VDD_IO	–	–	1	μA
	IIL2	VIL2=VSS	-200	-15	-1	μA
Input current 3 (P00-P07, P10-P17)	IIH3	VIH3=VDD_IO (In pull down)	1	15	200	μA
	IIL3	VIL3=VSS (In pull down)	-200	-15	-1	μA
	IIH3Z	VIH3=VDD_IO (at high impedance)	–	–	1	μA
	IIL3Z	VIL3=VSS (at high impedance)	-1	–	–	μA
Input voltage 1 (RESET_N, TEST0, TEST1_N, P00-P07, P10-P17)	VIH1	–	0.75× V_{DD_IO}	–	V_{DD_IO}	V
	VIL1	–	0	–	0.3× V_{DD_IO}	V
Input pin capacitance (RESET_N, TEST0, TEST1_N, P00-P07, P10-P17)	CIN	f=10kHz Vrms=50mV Ta=25°C	–	10	–	pF

Typ. standard is at Ta=25°C, VDD_IO=3.0V

6.13 Current consumption

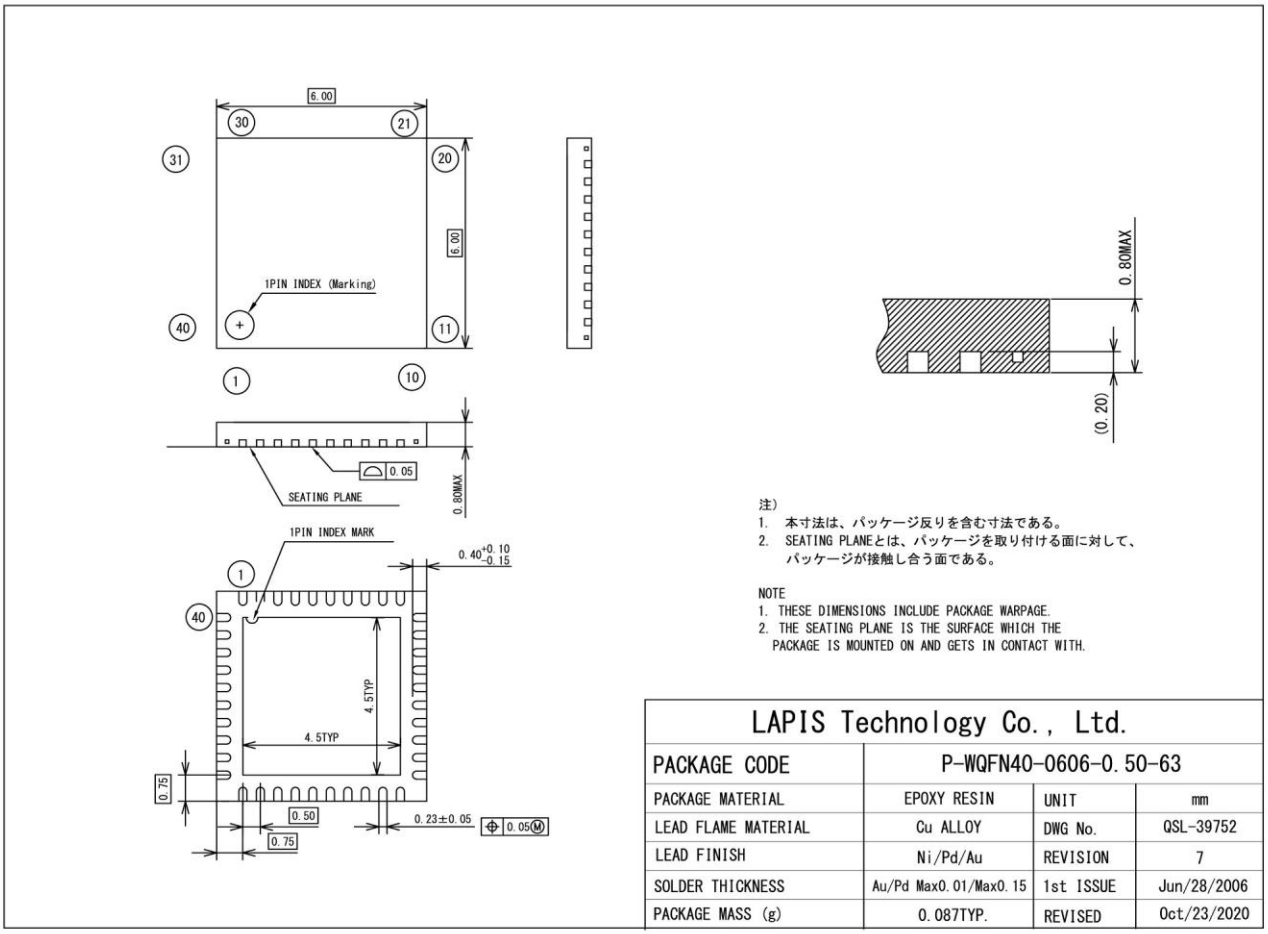
(VDD_IO=1.8 to 5.5V, P_EXT=4.5 to 5.5V, VSS=0V, Ta=-40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption	IDD1	HALT-H High speed clock stop	–	7	23.6	uA
	IDD2	HALT	–	1.3	2.0	mA
	IDD3	CPU 6.78MHz operation Peripherals stop	–	2.2	3.0	mA
	IDD4	CPU 6.78MHz operation Communication*	–	15	–	mA
	IDD5	CPU 6.78MHz operation Power transmission*	–	20	–	mA

* Current consumption depends on the antenna design. The smaller the load resistance, the higher the current consumption. External Transistor is not included.

7. Package dimensions

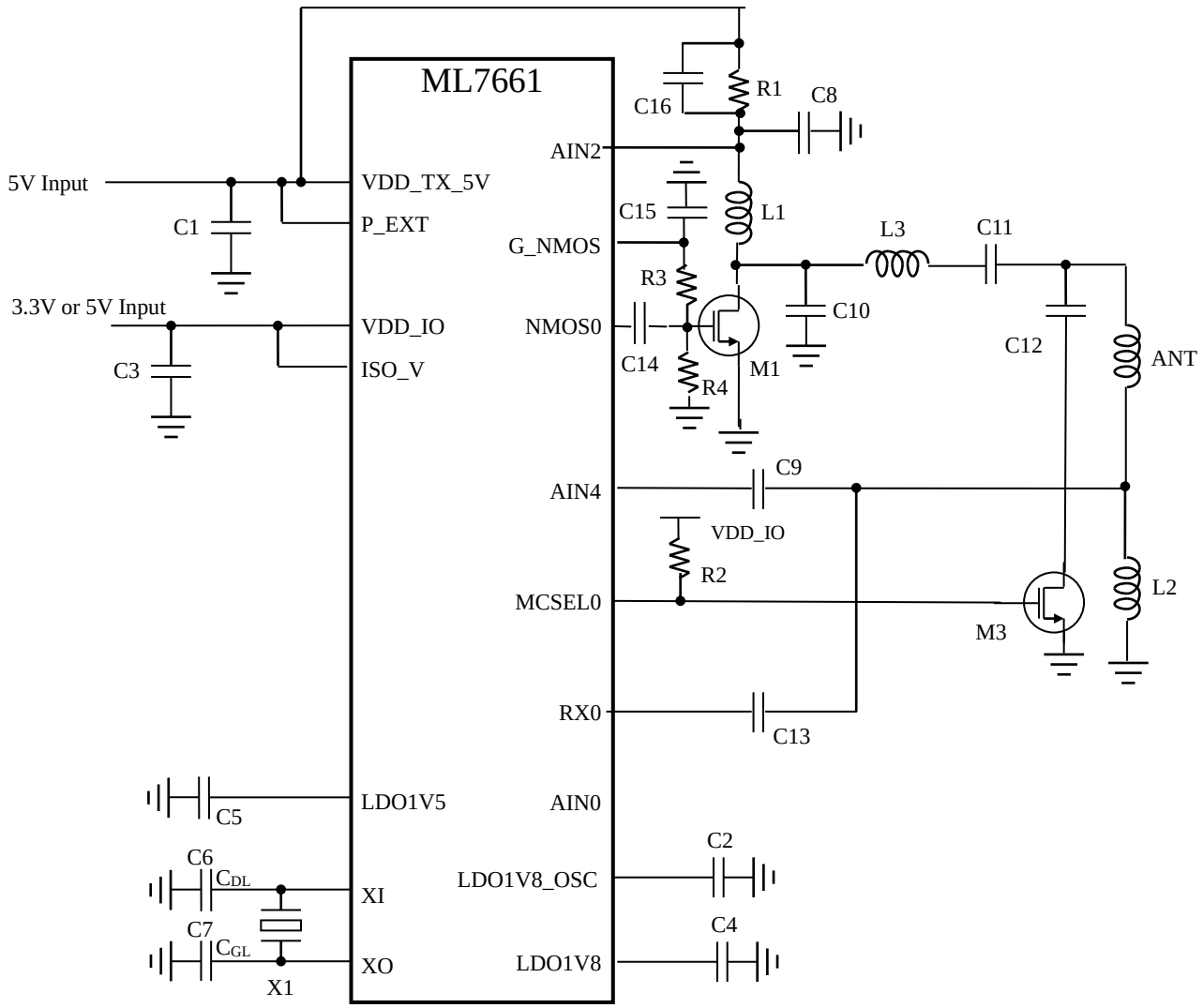
WQFN40 pin



LAPIS Technology Co., Ltd.			
PACKAGE CODE	P-WQFN40-0606-0.50-63		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-39752
LEAD FINISH	Ni/Pd/Au	REVISION	7
SOLDER THICKNESS	Au/Pd Max0.01/Max0.15	1st ISSUE	Jun/28/2006
PACKAGE MASS (g)	0.087TYP.	REVISED	Oct/23/2020

Notes for Mounting the Surface Mount Type Package
The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

8. Sample circuit



Mandatory Parts List

Parts Name	Parts Number	Value	Size	Manufacturer	Description
Inductor	L1	1µH	2016	Murata	LQM2MPN Series
	L2	22000pF	1005	Murata	GRM155 Series
	L3	240nH	2016	Murata	LQM2MPN Series
Capacitor	C6, C7	8pF	1005	Murata	GRM155 Series
	C12	15pF, over 100V	1005	Murata	GRM155 Series
	C11	100pF, over 100V	1005	Murata	GRM155 Series
	C8, C16	100pF	1005	Murata	GRM155 Series
	C10	120pF, over 100V	1005	Murata	GRM155 Series
	C2, C4	0.47µF	1005	Murata	GRM155 Series
	C1, C3, C5	2.2µF	1005	Murata	GRM155 Series
	C9, C13	560pF	1005	Murata	GRM155 Series
	C14	1000pF, DC cut	1005	Murata	GRM155 Series
	C15	1000pF	1005	Murata	GRM155 Series
Resistor	R1	47mΩ	1220	ROHM	LTR10 Series
	R2	1MΩ	1005	ROHM	MCR01 Series
	R3	51Ω	1005	ROHM	MCR01 Series
	R4	510Ω	1005	ROHM	MCR01 Series
MOS Transistor	M1	NMOS, 30V, 3.5A, 1W	2928	ROHM	RQ5E035BN
	M3	NMOS, 60V, 0.25A	2924	ROHM	RK7002BM
Crystal	X1	27.12MHz, 8pF	2016	NDK, Kyocera, TXC	NX2016SA, CX2016DB, SMD SEAM SEALING
ANT	-	-	-	-	-

Revision history

Document No.	Issue Date	Page		Change contents
		Previous Edition	Current Edition	
FEDL7661-01	2021.10.5	–	–	First edition

Notes

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